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Attorney's Docket No. ZILG.183US0
MAJESTIC, PARSONS, SIEBERT & HSUE
Four Embarcadero Center, Suite 1100
San Francisco, California 94111-4106
(415) 248-5500

CERTIFICATE OF EXPRESS MAILING UNDER 37 C.F.R. 1.10

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Name: Ken Lam

Signature: Ken Lam

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): Anatoliy V. Tsyrganovich

For: Circle Correction in Digital Low-Pass Filter

Enclosed are:

- [X] Eight sheets of [ ] formal/ [X] informal drawings.
- [X] An oath or declaration.
- [X] A power of attorney.
- [ ] A verification of small entity status.
- [X] An assignment of the invention to Zilog, Incorporated, Form PTO-1595 and a check in the amount of $40.00 to cover the fee.
- [ ] A certified copy of a _____ application.
- [X] A disclosure statement, PTO-1449 and copies of the references.

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(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) BASIC FEE $770.00
TOTAL CLAIMS	29 - 20 =	9	x $22.00	198.00
INDEPENDENT CLAIMS	6 - 3 =	3	x $80.00	240.00
MULTIPLE DEPENDENT CLAIMS FEE (if applicable)			x $260.00	
			SUBTOTAL FILING FEE	1208.00
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Joseph P. O'Malley, Reg.No. 36,226

TRANSMITTAL OF NEW PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR PATENT

CIRCLE CORRECTION IN DIGITAL LOW-PASS FILTER

Inventor: Anatoliy V. Tsyrganovich

Background of the Invention

The present invention relates to digital filters, especially digital low-pass filters for use with graphics encoders for video signals.

Figure 1 is a diagram of an example of a prior art digital filter 10. The digital filter 10 uses delay elements 12, 14, 16, 18 and 20, and summer 22. Such a digital filter produces an output defined by the equation

$$output(n) = g_1 input(n) + g_2 input(n-1) + g_3 input(n-2)$$

Any input is filtered in this prior art digital filter. It is desired to have an improved digital filter system.

Summary of the Preferred Embodiment

As described in the book "Video Demystified," Second Edition, by Keith Jack, incorporated herein by reference, digital video encoders typically use digital filters. In video encoders, the video pixel data can be defined in the Hue-Saturation-Intensity color space. The intensity corresponds to the black and white picture; the hue indicates the color, such as red or blue; and the saturation is an indication of the value of the color. A color with the same hue can have different saturation values; the same hue can range from pink to a dark red.

The most common television standards are the National Television Standards Committee (NTSC) standard used in the United States and the Phase Alternation Line (PAL) standard used in many European countries. Both of these standards derive from earlier standards in which all of the picture data is used to encode the black and white picture or luminance.

The color (hue and saturation) information is encoded onto a chrominance subcarrier about a subcarrier frequency within the picture data bandwidth. The chrominance subcarrier has a phase which encodes hue information and an amplitude which encodes saturation information.

In some situations, as described in the co-pending application of the same inventor entitled "Reduction of Color Transition Distortions in NTSC/PAL Encoder," incorporated herein by reference, it is beneficial to use the hue phase change between the pixel values which gives the minimum absolute value of the phase change. For example, a phase change from $\frac{1}{4}\pi$ to $7/4\pi$ produces a $3/2\pi$ phase change. By using the phase change from $\frac{1}{4}\pi$ to $-\frac{1}{4}\pi$ instead, the change in the hue is only $-\frac{1}{2}\pi$ and the color distortion between pixels is reduced.

A difficulty with this method concerns a hue signal simply reconstructed using the modified phase values. A large number of consecutive positive or negative modified phase change values can be produced. This would require a large number of bits for the reconstructed hue.

One embodiment of the present invention is the use of a correction signal which is a $2\pi n$ offset, n being an integer, added to the hue signals in order to keep the hue signals bounded. The $2\pi n$ correction signal does not affect the value of hue, since the hue values are encoded as a phase.

Another embodiment of the present invention is the use of a special filter for the hue signal that does not filter the $2\pi n$ correction components. A normal filter would filter the 2π step change component of the correction signal and produce spurious phase (color) values in the output video signal.

Another embodiment of the present invention is a digital filter that includes an unfiltered correction. In a preferred embodiment, the unfiltered correction is added by a summer in coefficient circuitry of the filter, and does not pass through an input delay line of the digital filter.

Brief Description of the Drawings

The above and other features and aspects of the present invention will become more apparent upon reading the following detailed description in conjunction with the accompanying drawings, in which:

Figure 1 is a diagram of a prior art digital filter;

Figure 2 is a diagram of a digital filter of the present invention using an unfiltered correction input;

Figure 3 is a diagram of an encoder for a video signal;

Figure 4 is a diagram of the filter of the present invention for use with the encoder of Figure 3;

Figure 5 is a digital phase circuitry for use with the filter of Figure 4;

Figure 6A is a graph of an input phase signal;

Figure 6B is a graph of a differential phase signal;

Figure 6 is an input to the phase corrector circuitry;

Figure 6D is a graph of the correction pulse;

Figure 6E is a graph of the filtered output of the circuit of the present invention;

Figure 7 is a graph of a circuit correction diagram in the polar representation; and

Figure 8 is a diagram of an alternate embodiment of the digital filter of the present invention.

Detailed Description of the Preferred Embodiment

Figure 2 is a diagram of the filter 30 of the present invention. The filter 30 includes an input delay line composed of digital delays 32 and 34. The signal from the delay lines goes to the coefficient circuitry 36, 38 and 40. Additionally, a correction input along lines 42 is sent to the coefficient circuitry 36, 38 and 40. The correction input on line 42 is not sent through the delays 32 or 34. In the correction circuitry, an adder 36a, 38a and 40a adds the correction input together with the input from the delay line. Additionally, since the correction input and main input are differential inputs, the output of the addition circuitry 36a, 38a and 40a is feedback after a delay as an input to the addition circuitry. The output of the delay 36b, 38b, and 40b is also sent to the gain amplifier 36c, 38c and 40c. The output of coefficient circuitry 36, 38 and 40 is sent to adder 42, which produces the filter output. Note that, since the correction input along line 42 is not sent through any of the delays 32 or 34, the correction input is not filtered. The correction input, however, is converted from a differential input and given a gain equal to $(G_1+G_2+G_3)$. By sending the correction input through the adders 36a, 38a and 40a, the correction input is given with the same gain as the delayed input. The circuitry could also be set up such that the gains G_1, G_2 and G_3

can be modified and the correction input need not be changed.

The main input and correction input in Figure 2 are both differential inputs. As shown in Figures 4-5, a differential input filter allows the improved differential hue circuitry of Figure 5 to be used.

Figure 3 is a diagram of a video encoder 50 that uses the filter of the present invention. A lookup table 52 converts red/green/blue (RGB) pixel data into hue saturation and intensity values. These values are filtered in filters 54 and sent to the additional PAL/NTSC encoding circuitry 56. The additional PAL/NTSC encoding circuitry 56 uses the saturation and hue values to produce a chrominance subcarrier which is added to the intensity values to produce the video signal. The vertical and horizontal blanking interval, audio, and other information is added to the video signal. Circuitry 58, the phase analysis element and low-pass filter, includes an embodiment of the filter of the present invention.

Figure 4 illustrates a preferred embodiment of the circuitry 50 of the present invention. The circuitry 50 includes differential phase circuitry 60 which converts the hue input into a differential phase output, along with the special filter 62 of the present invention. Also shown is the correction signal circuitry 54 used to produce the unfiltered correction signal for the filter 62.

A preferred embodiment of the differential phase circuitry 60 is shown in Figure 5. The differential phase circuitry is also discussed and claimed in a co-pending application entitled "Reduction of Color Transition Distortions in NTSC/PAL Encoder" by inventor Anatoliy V. Tsyrganovich. Also incorporated by reference is the co-pending application "Dot Crawl

Reduction in NTSC/PAL Graphic Encoder," by inventor Anatoliy V. Tsyrganovich.

Looking again at Figure 4, the differential phase circuitry 60 produces a modified differential phase. A simple reconstruction of the hue using the modified differential phase produces a hue value having unbounded values. The correction signal circuitry 64 and filter 62 is used to provide boundaries for the hue signal. When the hue value on line 66 is greater than a high reference value, the comparator 68 controls multiplexer 70 to output a -2π correction value on line 74. When the hue value on line 66 is less than a low reference value, comparator 72 controls multiplexer 70 to output a 2π correction value on line 74. If the hue value on line 66 is in between the high reference and the low reference values, the multiplexer 70 outputs zero as the correction value along line 74. In this manner, the hue output value is maintained within a desired boundary. In a preferred embodiment, the high reference value is 2π and the low reference value is zero. Thus, the hue output range only needs guard bands equal in width to the reference value discussed below with respect to the differential phase circuitry 60. Thus, in one embodiment, the guard bands range from 2π to 3π and 0 to $-\pi$ are used and the hue output is encoded within the range 3π to $-\pi$.

Note that the hue signal on line 66 is, in effect, an unfiltered reconstructed hue signal, since the differential hue, differential correction signal, and the last output of the addition circuitry 76a are added in addition circuitry 76a. The hue input is filtered, but the correction offset is not filtered. The correction offset does not pass through the input delay line but goes directly to the coefficient circuitry 76, 78 and 80.

Figure 5 is a graph of the differential phase circuitry 60. This circuitry 60 uses differential circuitry 90 to provide a differential or delta hue signal. This delta hue signal is modified in circuitry 92 to produce the modified delta hue output. The absolute value of the delta hue is compared to a reference value. If the absolute value of the delta hue is greater than a reference value, then a modified value is sent through multiplexer 94 to be added to the delta hue in adder 96 to produce the modified delta hue output.

Figure 6A is a graph of the phase in signal along line 61 of the differential phase circuitry 60 of Figure 4. Figure 6B is a graph of the differential signal output along line 63 of the differential phase circuitry 60 of Figure 4. Note that at a time T_1, the phase input moves up $3/2\pi$ in Figure 6A; however, the differential signal output drops down to produce a $-\frac{1}{2}\pi$ differential signal rather than a positive $3/2\pi$ differential signal. Figure 6C shows the input of the phase corrector circuitry 64 at line 66 in Figure 4. Note that, at time T_1, the phase corrector signal drops to zero rather than rising to 2π; zero and 2π being equivalent phases. At time T_2, the phase signal at line 66 drops down to $-\frac{1}{2}\pi$. Since this is less than the low reference value, comparator 72 and multiplexer 70 cause a positive 2π correction pulse at time T_3, as shown in Figure 6D.

Figure 6E shows the filter output at line 87 of Figure 4. Note that the filter acts as a low-pass filter to the input phase from line 66, as long as there is no correction pulse. At time T_3, a correction pulse is produced which is not filtered by the circuitry 62. The output jumps up to a corresponding value within the range 0 to 2π, and continues low-pass filtering the transition. If the correction pulse component was

filtered, as shown in phantom line 100, spurious values for the color of the pixel location would be produced. Note that the value 102 is an equivalent phase representation to the value 104 which is the filtered output that would be produced if there is no correction pulse.

Figure 7 is a graph illustrating a circle correction for a virtual polar representation. As shown in Figure 7, there is a main phase range 110 from zero to 2π. Guard band 112 ranges from 2π to 3π, and guard band 114 ranges from 0 to $-\pi$. Note that the values in the guard bands 112 and 114 correspond to values within the main range 110, thus allowing a positive or negative 2π jump onto the main phase range 110.

Figure 8 is an alternate embodiment of the filter of the present invention. This alternate embodiment of the filter 120 includes the delay lines 122 and 124, coefficient circuitry 126, 128 and 130, summer 132 and the integration circuitry 134. Integration circuitry 134 converts the differential correction signal at point 136 to a correction offset level at point 138. The adder 126a, 128a and 130a adds the correction offset 138 with the output of the delay line including delays 122 and 124. The correction offset 138 is not filtered, while the input at line 121 is filtered. The output can be given by the equation

$$output(n)=g_1(input(n)+offset(n))+\ g_2(input(n-1)+offset(n))\ +\ g_3(input(n-2)+offset(n))$$

which reduces to

$$output(n)\ =\ g_1 input(n)+\ g_2 input(n-1)\ +\ g_3 input(n-2)+g_t offset(n)$$

where

$$g_t=g_1+g_2+g_3$$

When g_t is equal to 1, the output of the filter of Figure 8 is equal to the filtered input value on 121 plus the offset value at 138.

Various details of the implementation and method are merely illustrative of the invention. It will be understood that various changes in such details may be within the scope of the invention, which is to be limited only by the appended claims.

WHAT IS CLAIMED IS:

1. A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered.

2. The circuit of claim 1, wherein the first circuit portion is a delay line.

3. The circuit of claim 1, wherein the second circuit includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input.

4. The circuit of claim 3, wherein the output of the at least one coefficient circuits is to a delay and the output of delay sent to the at least one coefficient circuits.

5. The circuit of claim 3, wherein the coefficient circuit includes an input summer and a coefficient multiplier.

6. The circuit of claim 3, further comprising a summer circuit to add the outputs of the at least one coefficient circuit.

7. The circuit of claim 1, wherein the first input and output are phase representations and wherein the adjustment input causes an integer multiple of 2π shift in the output signal.

8. The circuit of claim 1, wherein the first input is differential phase input.

9. The circuit of claim 1, further comprising adjustment control logic adapted to provide the adjustment input.

10. The circuit of claim 9, wherein the adjustment control logic is adapted to produce a minus 2π adjustment signal if a tested signal is greater than a positive reference value and produce a positive 2π adjustment signal if the tested signal is less than a negative reference value.

11. The circuit of claim 1, wherein the second circuit portion is such that, when there is no adjustment input, the circuit acts as a filter as to the first input.

12. A circuit comprising:

a digital filter including input lines giving signal values at different time indexes, coefficient multiplier circuitry adapted to multiply the signal values by filter coefficients, and a summer connected to the coefficient multiplier circuitry to produce an output value; and

summing circuitry connected to the input lines of the signal values at different time indexes and to an adjustment input, wherein the output of the summing circuitry being sent to the coefficient multiplying circuitry.

13. A method comprising:

providing a circuit;

inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit; and

inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset to the output.

14. The method of claim 13, wherein the adjustment signal keeps the output within a preset range.

15. The method of claim 13, wherein the filtering of the input signal is a low-pass filtering.

16. The method of claim 13, wherein the input is a phase signal.

17. The method of claim 13, wherein the input is a hue signal.

18. A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal.

19. The method of claim 18, wherein the filtering of the modified phase signal is a low-pass filtering.

20. The method of claim 18, wherein the correction signal is an integer multiple of 2π.

21. The method of claim 18, wherein the preset range is zero to 2π.

22. The method of claim 18, wherein the preset range is zero to 2π plus a guard band.

23. The method of claim 22, wherein the guard band is a reference value above or below the range zero to 2π.

24. The method of claim 23, wherein the guard bands are $-\pi$ to zero and 2π to 3π.

25. The method of claim 18, wherein the constraining step is such that the phase signal is processed so as to use a differential input.

26. The method of claim 25, wherein the differential input is offset by an integer multiple of 2π so as to reduce the absolute value of the differential input.

27. The method of claim 18, wherein the phase signal is a hue signal.

28. An apparatus comprising:

circuitry to constrain a phase signal within a preset range using a correction signal; and

a filter adapted to filter the phase signal without filtering the correction signal contribution.

29. A method of processing data for video comprising:

providing picture data including hue information encoded as a phase having a first range;

producing a filtered hue information signal, the filtered hue information signal including unfiltered offsets of plus or minus 2π.

Abstract of the Disclosure

A filter circuit is provided which has a filtered input and an unfiltered input. The filtered input passes through delay elements to coefficient circuitry. The unfiltered input passes to the coefficient circuitry without passing through the delay elements. In this manner, an unfiltered offset can be added to the filtered output. This filter is especially useful when the filtered value is in phase representation form; for example, when the filter value is a hue value encoded as a phase.

PATENT APPLICATION DECLARATION

(Attorney's Docket No.: ZILG.183US0)

I, ANATOLIY V. TSYRGANOVICH, declare as follows:

1. My residence, post office address and country of citizenship given below are true and correct.

2. I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought in the attached patent application entitled "CIRCLE CORRECTION IN DIGITAL LOW-PASS FILTER," and I have reviewed and understand the contents of the specification, including its claims.

3. I acknowledge my duty to disclose to the Office all information known to me to be material to patentability of this application, in accordance with 37 C.F.R. Section 1.56, which is defined on the attached page.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Additionally, the undersigned hereby appoints the following as his attorneys and agents to prosecute said patent application, to transact all business in the Patent and Trademark Office connected therewith, to receive the original Letters Patent and to substitute or associate other attorneys on his behalf:

Gerald P. Parsons	Registration No. 24,486
Martin F. Majestic	Registration No. 25,695
J. Suzanne Siebert	Registration No. 28,758
James S. Hsue	Registration No. 29,545
Keiichi Nishimura	Registration No. 29,093
Philip Yau	Registration No. 32,892
Joseph P. O'Malley	Registration No. 36,226
George L. Fountain	Registration No. 36,374
K. Alison de Runtz	Registration No. 37,119

Please send all correspondence to:

Gerald P. Parsons, Esq.
MAJESTIC, PARSONS, SIEBERT & HSUE
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111-4106

Telephone: 415/248-5500
Facsimile: 415/362-5418

Date: 09/12/97

Residence and
Post Office Address:

ANATOLIY V. TSYRGANOVICH
906 Windsor Hills Circle
San Jose, California 95123
(Citizenship: Belarus)

Section 1.56 Duty to Disclose Information Material to Patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

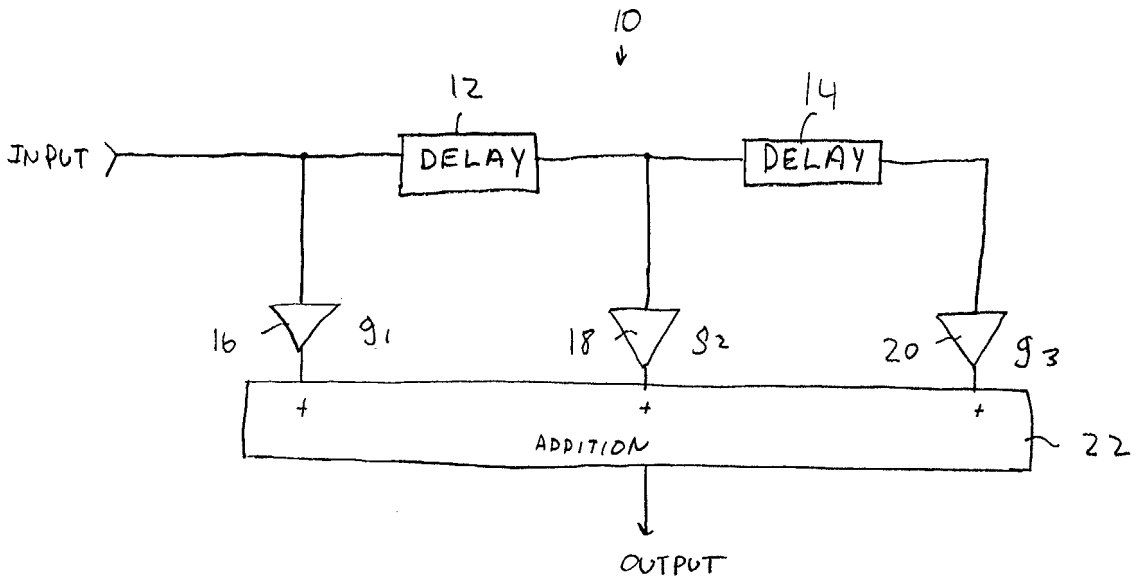


FIGURE 1
(PRIOR ART)

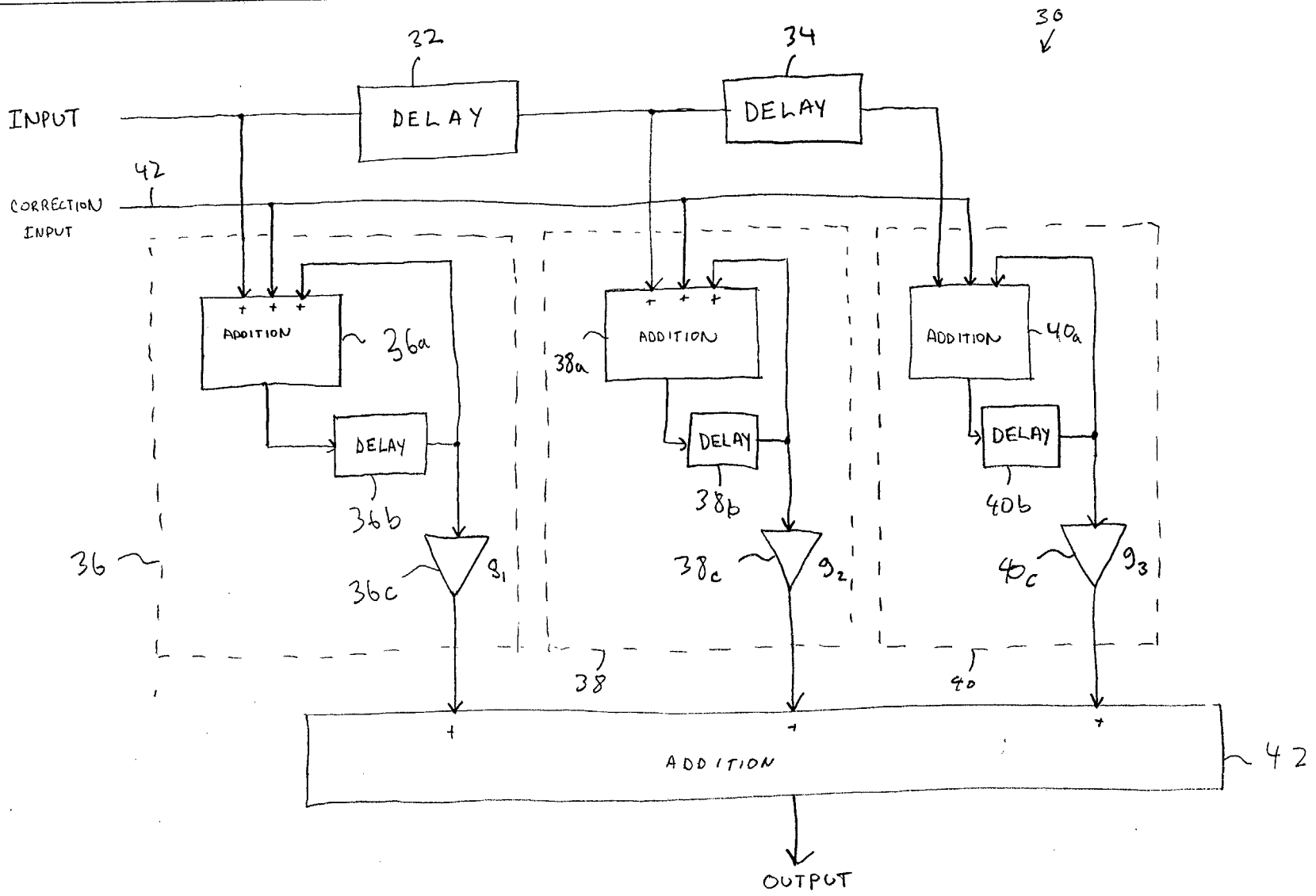


FIGURE 2

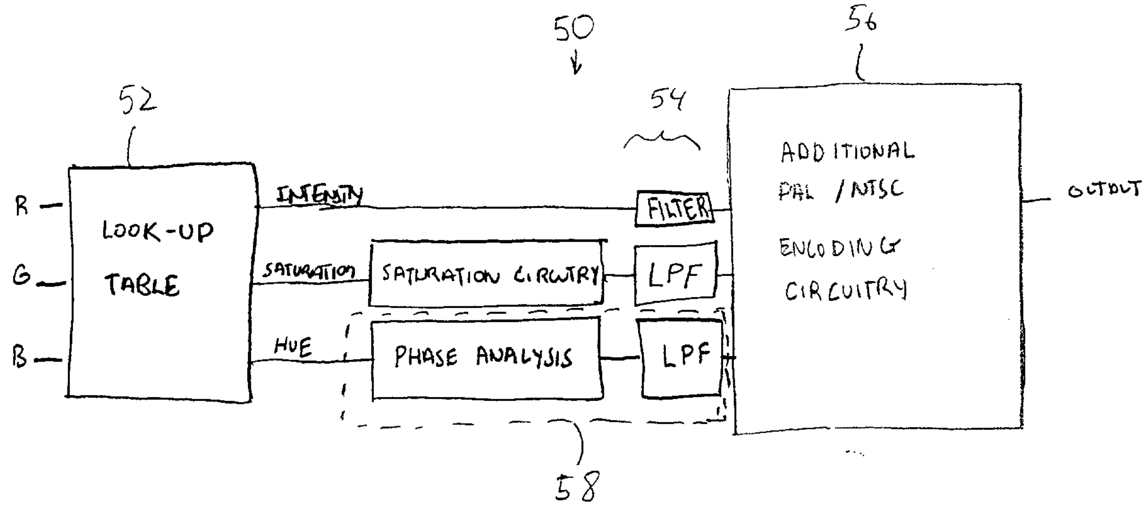

50
52
54
56
R
G
B
LOOK-UP TABLE
INTENSITY
SATURATION
HUE
FILTER
SATURATION CIRCUITRY
LPF
PHASE ANALYSIS
LPF
ADDITIONAL PAL / NTSC ENCODING CIRCUITRY
OUTPUT
58

FIGURE 3

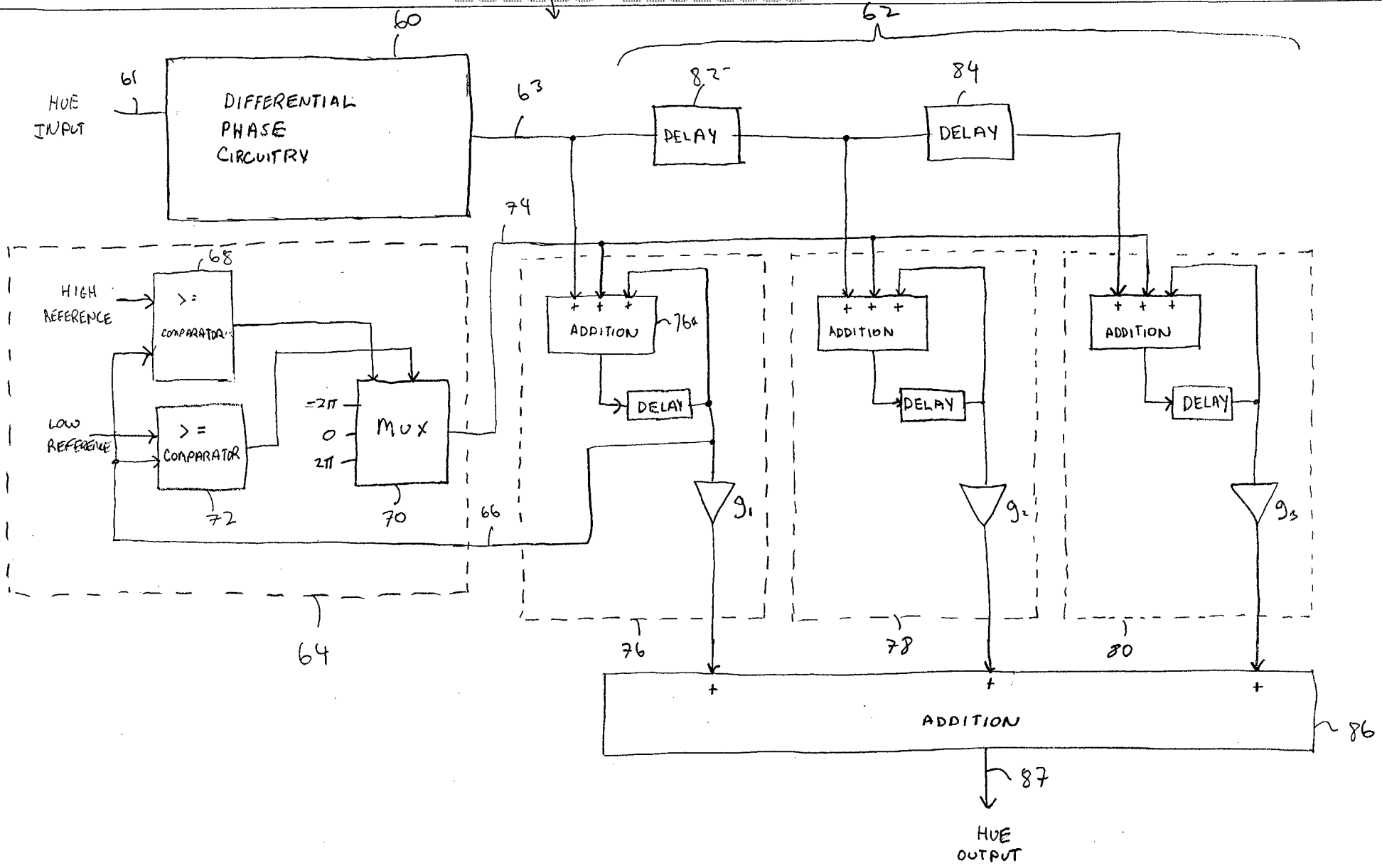


FIGURE 4

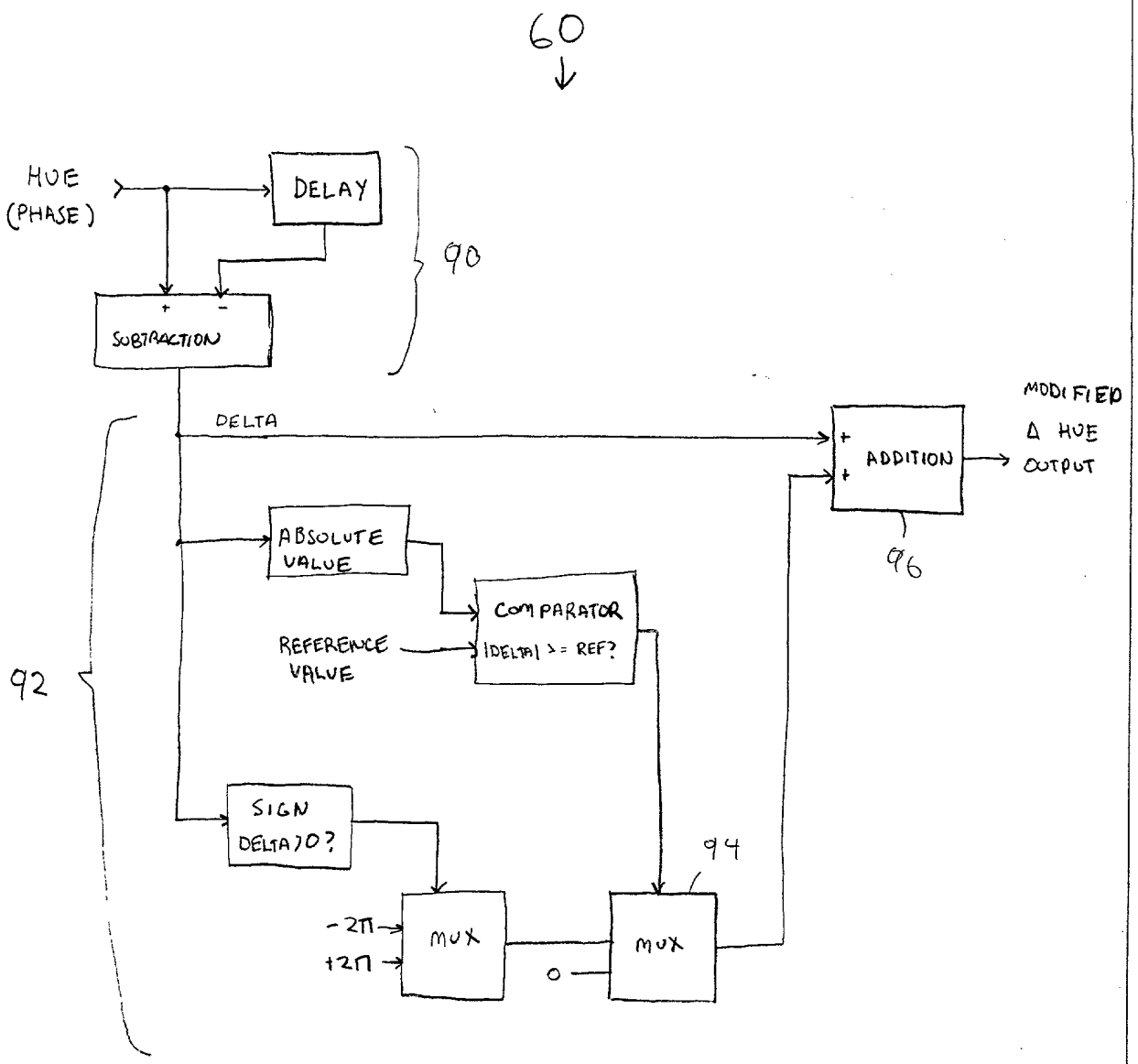

60
HUE
(PHASE)
DELAY
90
SUBTRACTION
+
−
DELTA
ADDITION
+
+
MODIFIED
Δ HUE
OUTPUT
96
ABSOLUTE
VALUE
COMPARATOR
|DELTA| >= REF?
REFERENCE
VALUE
92
SIGN
DELTA>0?
94
-2π
+2π
MUX
MUX
0

FIG. 5

FIG. 6A

PHASE IN

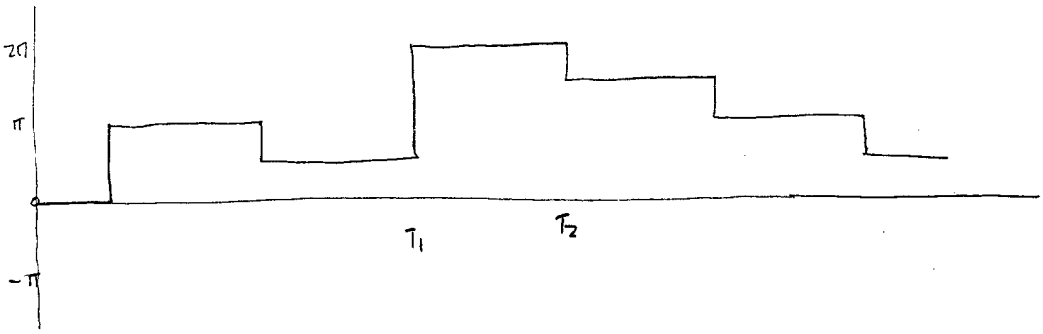


FIG. 6B

DIFFERENTIAL SIGNAL

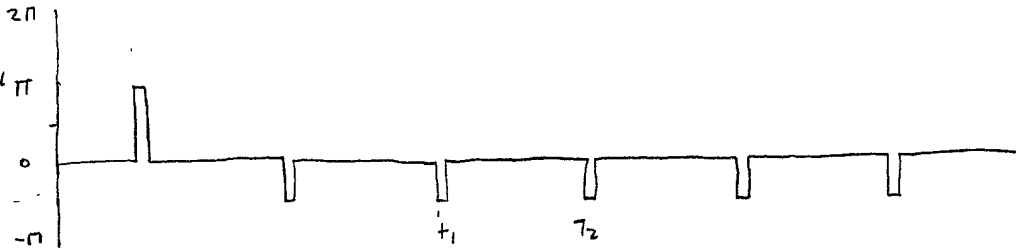


FIG. 6C

INPUT OF PHASE CORRECTOR

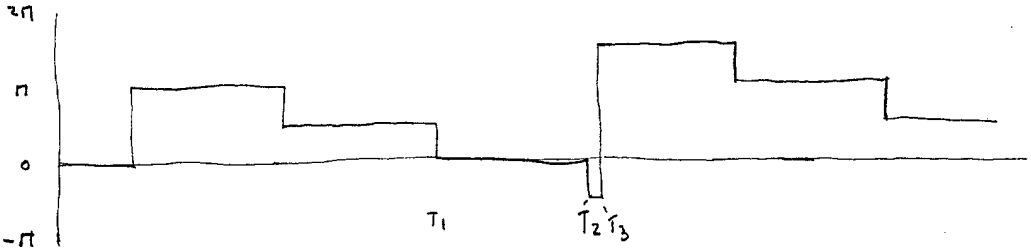


FIG. 6D

CORRECTION PULSE

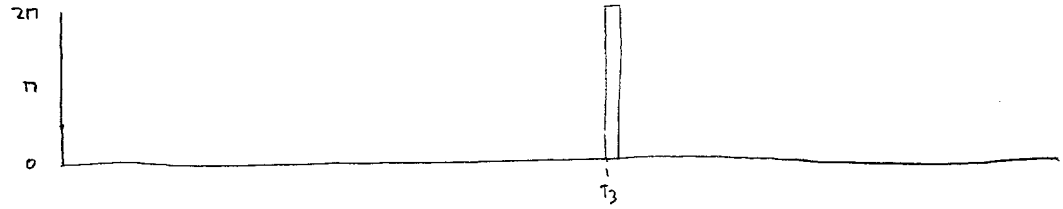
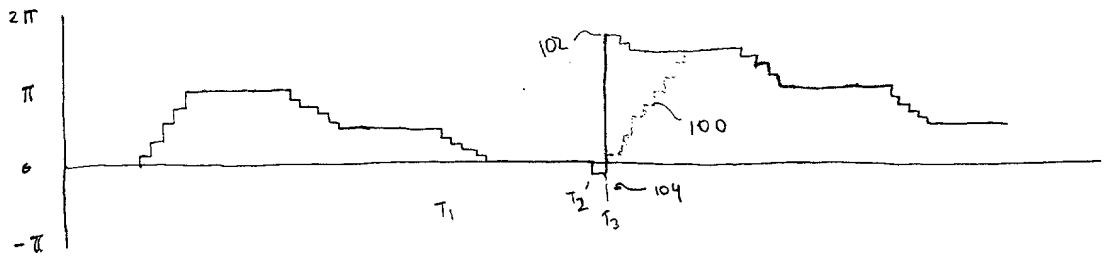


FIG. 6E

FILTER OUTPUT



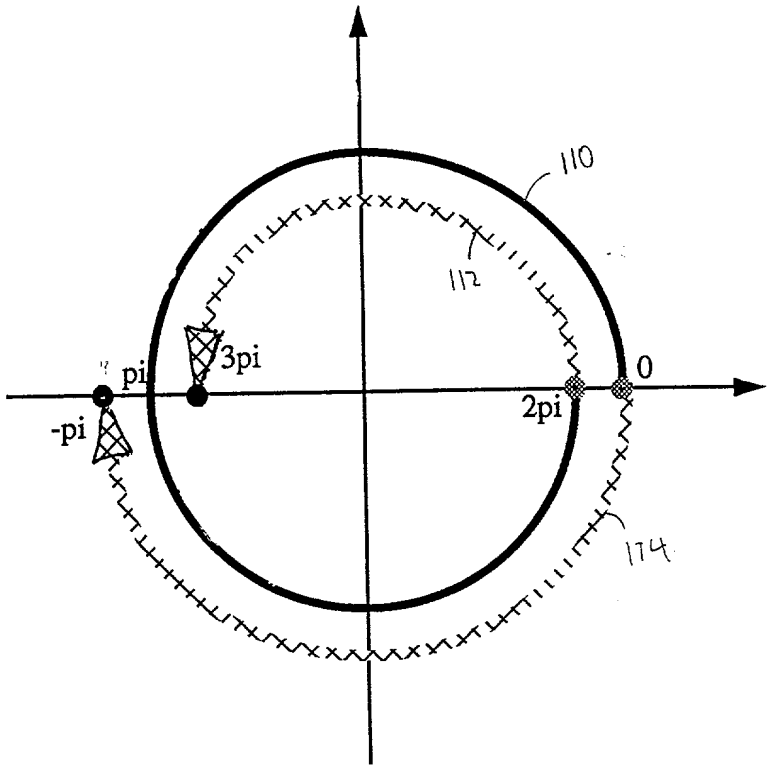


FIG. 7

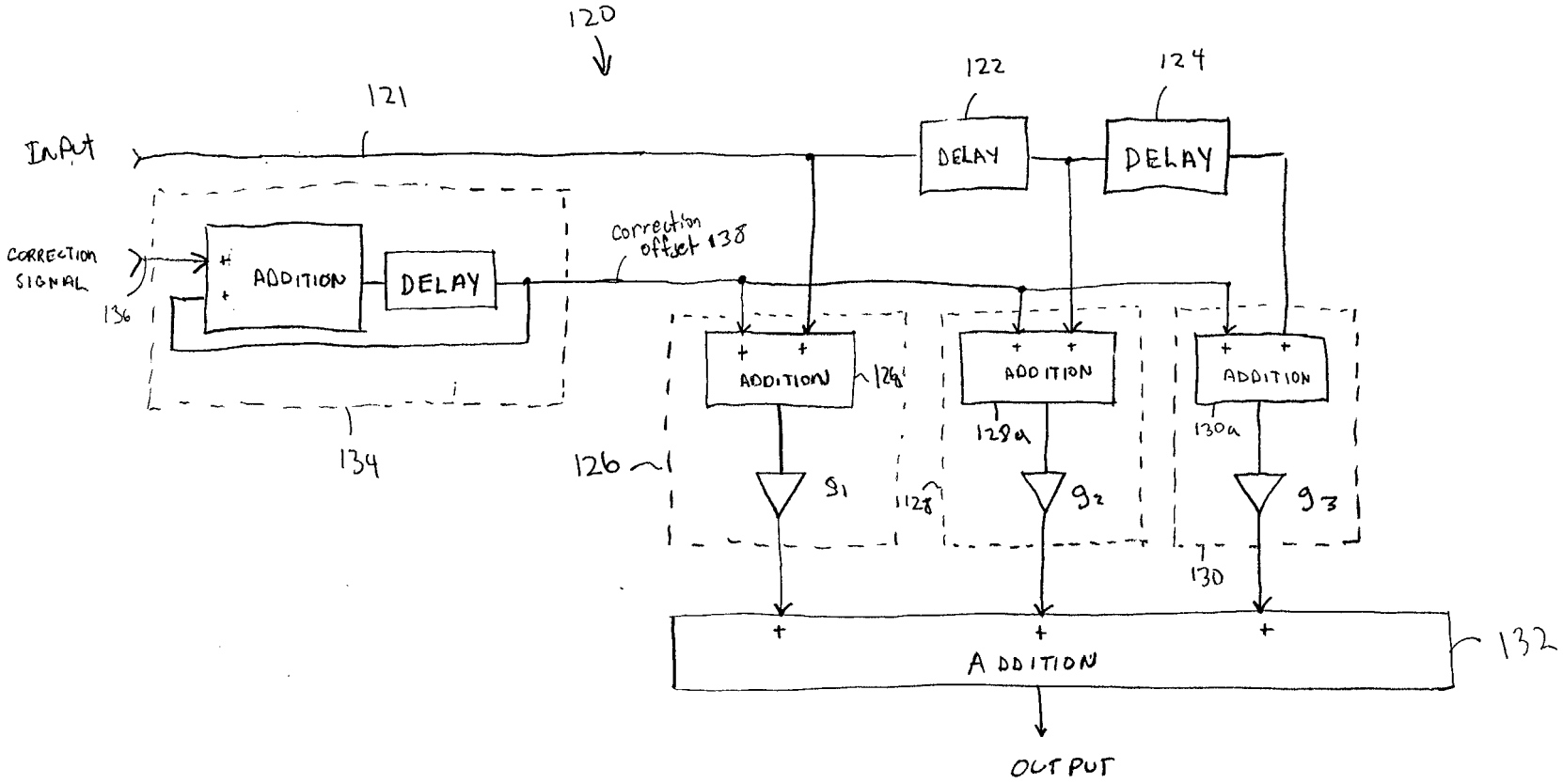


FIG. 8